I Claim:

1. An apparatus for effecting a controlled startup of a processor device; the apparatus comprising:

(a) a first signal-treating circuit coupled with a voltage supply locus; said first signal-treating circuit receiving a voltage supply signal and producing a first treated signal representing said voltage supply signal;

(b) a second signal-treating circuit coupled with said voltage supply locus; said second signal-treating circuit receiving said voltage supply signal and producing a second treated signal representing said voltage supply signal; and

(c) a comparing unit; said comparing unit having a first input locus coupled with said first signal-treating circuit and receiving said first treated signal; said comparing unit having a second input locus coupled with said second signal-treating circuit and receiving said second treated signal; said comparing unit generating an output signal at an output locus when said first treated signal has a predetermined relationship with said second treated signal; said output locus being coupled with said processor device; said output signal effecting said controlled startup.

2. An apparatus for effecting a controlled startup of a processor device as recited in Claim 1 wherein said processor device includes a reset control pin; signals applied to said reset control pin controlling a reset operation of said processor device; said output locus being coupled with said reset control pin.

3. An apparatus for effecting a controlled startup of a processor device as recited in Claim 1 wherein said first treated signal is a time-delayed representation of said voltage supply signal and wherein said second treated signal is a non-delayed representation of said voltage supply signal.

4. An apparatus for effecting a controlled startup of a processor device as recited in Claim 2 wherein said first treated signal is a time-delayed representation of said

voltage supply signal and wherein said second treated signal is a non-delayed representation of said voltage supply signal.

5. An apparatus for effecting a controlled startup of a processor device as recited in Claim 1 wherein said comparing unit is a comparator.

6. An apparatus for effecting a controlled startup of a processor device as recited in Claim 5 wherein said processor device includes a reset control pin; signals applied to said reset control pin controlling a reset operation of said processor device; said output locus being coupled with said reset control pin.

7. An apparatus for effecting a controlled startup of a processor device as recited in Claim 5 wherein said first treated signal is a time-delayed representation of said voltage supply signal and wherein said second treated signal is a non-delayed representation of said voltage supply signal.

8. An apparatus for effecting a controlled startup of a processor device as recited in Claim 6 wherein said first treated signal is a time-delayed representation of said voltage supply signal and wherein said second treated signal is a non-delayed representation of said voltage supply signal.

9. An apparatus for controlling operation of a processor device during startup of said processor device; the apparatus comprising:

(a) a signal treating circuit receiving a voltage supply signal at a voltage supply locus; said signal treating circuit using said voltage supply signal for generating a first treated signal and a second treated signal; and

(b) an output circuit coupled with said signal treating circuit; said output circuit receiving said first treated signal and said second treated signal and generating a control signal at an output locus based upon a relationship between said first

treated signal and said second treated signal; said output locus being coupled with said processor device; said control signal effecting said controlling.

10. An apparatus for controlling operation of a processor device during startup of said processor device as recited in Claim 9 wherein said processor device includes a reset control pin; signals applied to said reset control pin controlling a reset operation of said processor device; said output locus being coupled with said reset control pin.

11. An apparatus for controlling operation of a processor device during startup of said processor device as recited in Claim 9 wherein said first treated signal is a time-delayed representation of said voltage supply signal and wherein said second treated signal is a non-delayed representation of said voltage supply signal.

12. An apparatus for controlling operation of a processor device during startup of said processor device as recited in Claim 10 wherein said first treated signal is a time-delayed representation of said voltage supply signal and wherein said second treated signal is a non-delayed representation of said voltage supply signal.

13. An apparatus for controlling operation of a processor device during startup of said processor device as recited in Claim 9 wherein said output circuit comprises a comparator.

14. An apparatus for controlling operation of a processor device during startup of said processor device as recited in Claim 13 wherein said processor device includes a reset control pin; signals applied to said reset control pin controlling a reset operation of said processor device; said output locus being coupled with said reset control pin.

15. An apparatus for controlling operation of a processor device during startup of said processor device as recited in Claim 13 wherein said first treated signal is a time-

delayed representation of said voltage supply signal and wherein said second treated signal is a non-delayed representation of said voltage supply signal.

16. An apparatus for controlling operation of a processor device during startup of said processor device as recited in Claim 14 wherein said first treated signal is a time-delayed representation of said voltage supply signal and wherein said second treated signal is a non-delayed representation of said voltage supply signal.

17. A method for controlling operation of a processor device during startup of said processor device; the method comprising the steps of:

(a) in no particular order:

(1) providing a signal treating circuit; and

(2) providing an output circuit coupled with said signal treating circuit;

(b) operating said signal treating circuit to receive a voltage supply signal at at least one voltage supply locus;

(c) operating said signal treating circuit to use said voltage supply signal for generating a first treated signal and a second treated signal;

(d) operating said output circuit to receive said first treated signal and said second treated signal;

(e) operating said output circuit to generate a control signal at an output locus; said control signal being based upon a relationship between said first treated signal and said second treated signal; and

(f) providing said control signal to said processor device for effecting said controlling.

18. A method for controlling operation of a processor device during startup of said processor device as recited in Claim 17 wherein said processor device includes a reset control pin; signals applied to said reset control pin controlling a reset operation of said processor device; said output locus being coupled with said reset control pin.

19. A method for controlling operation of a processor device during startup of said processor device as recited in Claim 18 wherein said output circuit comprises a comparator.

20. A method for controlling operation of a processor device during startup of said processor device as recited in Claim 19 wherein said first treated signal is a time-delayed representation of said voltage supply signal and wherein said second treated signal is a non-delayed representation of said voltage supply signal.